ADVANCED VEHICLE TECHNOLOGIES, Inc.

AVT-512

M-Module Interface

for Vehicle Networks

Hardware Revision "B"

User's Manual

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1. INTRODUCTION

This manual covers the AVT-512 M-Module Interface unit, hardware revision "B". It provides the following technical information, and more, about the interface:

- Configuration.
- Installation.
- Operations.
- Communications.
- Connections.

The AVT-512 M-Module Interface supports the following network protocols.

- CAN (Controller Area Network).
  2-wire support.
  GM Single Wire CAN (SWC) support.
- J1850 VPW
  GM Class 2 compliant.
- J1850 PWM
  Ford SCP compliant.
- Keyword Protocol 2000 support (K-line only)
  ISO 14230 and ISO 9141.
- Ford UBP (UART Based Protocol).

The AVT-512, order **# 512-001**, consists of the AVT-512 M-Module Interface board, a disk containing available VXI*plug&play* drivers (none available at the time of this writing), and relevant documentation on disk.

The AVT-512, order **# 512-002** consists of the AVT-512 M-Module Interface board and relevant documentation on disk.

The AVT-512 M-Module Interface conforms to the M-Module specification, ANSI/VITA 12-1996.

Operations in CAN mode are compatible with ISO-11898, J1939, J2411, and other specifications.

Operations in J1850 VPW mode conform to specification J1850 and GM Class 2 requirements.

Operations in J1850 PWM mode conform to specification J1850 and Ford SCP (Standard Corporate Protocol) requirements.

Operations in UBP mode conform to Ford Motor Company UBP requirements.

The AVT-512 M-Module Interface provides the following functions:

- Protocol/data conversion between a vehicle based network and the host computer (via memory mapped FIFOs).
- Active network node.
- Passive network traffic monitor.

1.1 Revision "B" Hardware

The current production hardware of the AVT-512 is revision "B". There were very few revision "A" units built and they are quite different from the revision "B" hardware. The most significant change with revision "B" was the incorporation of electrical isolation between the external vehicle networks and the host VXI electrical system.

A brief summary of the differences between revision "A" and "B" hardware is presented here.

- Revision "B" hardware provides full electrical isolation between the external vehicle networks and the host VXI system.
- Revision "B" hardware uses the Motorola HBCC device for J1850 PWM support [Ford SCP].
- Revision "B" hardware does not provide "L-line" support. [KWP2000 only]
- The interrupt vector DIP switch present on revision "A" has been removed.
- Revision "B" hardware provides the status register value on the upper 8-bits of the interrupt word. (The lower 8-bits are the logical address of the interrupting module.)

1.2 Cautionary Note

The AVT-512 revision "B" hardware provides full electrical isolation between the external vehicle network and the host VXI system. It is important that the user maintain this isolation.

> The user is strongly cautioned not to create any electrical connection, especially ground, between the external equipment under test and the host VXI system. Establishing an inadvertent ground connection can be easily overlooked and could result in costly damage to the host VXI system.

For example; the vehicle network connector on the AVT-512 is all plastic and is not connected to the host VXI system ground. However, the small stainless steel dress panel for that connector is usually clipped to the carrier board front panel and thus may be connected to the host VXI system ground.

Unknowingly attaching a connector with a grounded shell to the AVT-512 vehicle network connector may create a ground path from the external equipment under test to the host VXI system chassis ground. Damage to the host VXI system could result.

1.3 Specifications and Requirements

AVT-512 M-Module Interface

- Double wide M-Module.
- Overall size: 148.26 x 106.24 x 12.00 mm.
- Weight: 142 grams.
- +5 VDC from host.
- +12 VDC from host.
- +12 VDC, V-BATT, nominal battery, from vehicle (diode isolated from host +12 VDC supply and jumper selected).
- Input voltage range: +9.0 VDC to +30.0 VDC.
  (From external source, applied to +12 VDC input.)
- Power dissipation: 3.5 watts nominal, 4.0 watts peak.
  (Total for +5 VDC and +12 VDC supplies.)

1.4 Definitions

The following terms are used in this manual.

- CAN: Controller Area Network.
- CRC: Cyclic Redundancy Check.
- DLC: Data Link Controller. [Motorola term, VPW]
- HBCC: Hosted Bus Controller Chip: J1850 PWM controller/interface device. [Ford SCP device]
- KWP: Keyword Protocol 2000 (ISO 14230). [K-line only.]
- OBD-II: On Board Diagnostics, phase two.
- SCC: Serial Communications Controller. [A dual UART device]
- SCI: Serial Communications Interface. [Motorola term]
- SCP: Standard Corporate Protocol. [Ford Motor Company]
- SWC: Single Wire CAN. [J2411]
- UBP: UART Based Protocol. [Ford Motor Company unique]
- Most numbers used in this manual are hexadecimal digits (0 .. 9 and A .. F) and are usually preceded with a dollar sign ($) for clarity.

2. AVT-512 M-Module Installation

The AVT-512 must be configured, installed onto an M-Module carrier board, and then installed in the host VXI system. The AVT-512 is then connected to the external network (optional) and external V-BATT voltage source (optional).

Note that the AVT-512 is an M-Module designed to conform to ANSI/VITA 12-1996. It should work in any system capable of accommodating an M-Module. Though this document refers to the "host VXI" system, the AVT-512 is not constrained to VXI systems.

If other systems (cPCI, PXI, etc.) are M-Module compatible, and able to accommodate a double wide M-Module, then the AVT-512 may be used there as well.

2.1 Configuration

The AVT-512 M-Module has several jumpers on the board that should be configured before being installed onto the carrier board. These jumpers include configuration of the vehicle network connector (P3) and the +12 VDC power source. Refer to Sections 6.3.8, 6.3.9, and 6.3.10 for detailed information.

2.2 Installation - General

These installation instructions are for installing the AVT-512 M-Module onto an Agilent E2251A M-Module Carrier board. Other carrier boards should accommodate the AVT-512 M-Module, but the installation may be different - consult the appropriate manufacturers manuals for the M-Module carrier board being used.

2.3 Installation - Agilent E2251A Carrier

The Agilent E2251A M-Module carrier board will accommodate as many as six single wide M-Module units. The AVT-512 is a double wide M-Module. Any combination of M-Modules can be installed onto the Agilent E2251A M-Module carrier - within mechanical restrictions or constraints (e.g. the AVT-512 requires two adjacent M-Module slots).

There are two host connectors (P4 and P5) on the AVT-512. These are double row connectors with 20 positions per row. Only connector P5 is active. Connector P4 is not electrically used, it only provides additional ground connections. P4 is there to provide mechanical stability.

Since only connector P5 is active, when installed onto the carrier board the AVT-512 becomes active in the lower order slot of the two slots being occupied. For example, if installed into slots M1 and M2 of the carrier board, only slot M1 is active and is connected to the AVT-512.

Configure the AVT-512 M-Module jumpers.
Refer to Sections 6.3.8, 6.3.9, and 6.3.10 for detailed information.

Determine and set the Logical Address switches on the carrier board, for the lower order slot to be occupied by the AVT-512 (only connector P5 is active). Be sure to disable the higher order slot being occupied by the AVT-512 unit. (On the Agilent E2251A setting the logical address to $00 disables that slot.)

Two dress panels are provided with the AVT-512. These dress panels were designed to fit the Agilent E2251A M-Module carrier board. One dress panel is punched for vehicle network connector P3 (a DA-15P connector) and for the two status LEDs.

Remove the jack screws on P3, install the dress panel, and re-install the jackscrews. The bent edge of the dress panel should hang over the connector. It will mate to the carrier board front panel.

Carefully install the AVT-512 onto the carrier board. Be sure to carefully line up the pins and connectors for the two carrier board connectors. It is recommended that vehicle network connector P3 is placed through the carrier board front panel, then line up connectors P4 and P5 to the carrier board, seat P4 and P5, and then fully seat the dress panel to the carrier board front panel.

The remaining dress panel is blank and is used to cover the other M-Module slot occupied by the AVT-512 unit.

Re-assemble the M-Module carrier board (covers and shields) and re-install it into the host chassis.

2.4 Connections

The AVT-512 front panel vehicle network connector, P3, provides all connections to the external vehicle networks and power supply (optional). Refer to Section 6.3.12 for a detailed description of P3. Note that the configuration for P3 is affected by the jumpers on JP1.

If connected, the external power source should be a nominal +12 VDC minimum of +9.0 VDC and maximum of +30.0 VDC. Supply voltage above this range may result in harm to the AVT-512 and possibly blow fuse F4; thus resulting in operational failures.

2.5 Power-on Observations

When power is applied to the AVT-512 M-Module it will immediately come up running in an idle state. All external networks are disconnected and all modes of operation are disabled. The green LED should be lit and the red LED should be blinking fast.

2.6 Verifying Communications

The AVT-512 M-Module is a memory mapped device. Refer to Section 4.2.1 for a detailed description of the various registers defined for the AVT-512.

Access to the AVT-512 can be done through direct memory/register I/O or by using the VXI*plug&play* drivers. [VXI*plug&play* drivers are under development at the time of this writing. Consult the AVT web site or contact the factory for the latest information regarding the availability of VXI*plug&play* drivers.]

An Agilent VEE program is available from the factory that implements a basic hex terminal function for the AVT-512 M-Module Interface - running in Agilent VEE. It provides a quick way to test the installation and operation of the AVT-512 M-Module Interface. Contact the factory to obtain a copy of the software.

Also available from the factory is a Visual Basic 6.0 program that implements a basic hex terminal function for the AVT-512 M-Module Interface. That program uses the Agilent Resource Manager and Agilent VISA DLL functions to communicate with the AVT-512 board. Contact the factory to obtain a copy of the software.

Using an AVT-512 hex terminal software application (or any other software providing a similar function), the installation and operation of the AVT-512 can be quickly verified. Within one-half second of power-on, the AVT-512 makes available in FIFO #2 the following bytes:
$91 $12 and $92 $04 $xx.

Explanation:
$91 $12 - indicates that the AVT-512 board is running in the idle power-on state awaiting a mode switch command.
$91 $04 $xx - is a firmware version report where "xx" is the version number of the firmware running on the AVT-512 board.

Refer to Section 5.0 for more detailed information on communications between the AVT-512 and the host computer.

These reports read from the AVT-512 provide a reasonable indication of confidence that the AVT-512 is installed correctly and operating properly. The user can issue commands to the AVT-512 at this point and observe proper responses thus indicating properly functioning of communications with the AVT-512 M-Module Interface.

3. AVT-512 M-Module Interface Hardware

The following sections provide a brief description of the hardware implementation of the AVT-512 M-Module Interface. A block diagram of the AVT-512 is shown in Figure 1.

Included on the block diagram are all signal assignments and pin numbers for JP1 and P3.

3.1 Introduction

The AVT-512 M-Module Interface provides a communications interface between the host VXI system and any of the automotive computer network protocols supported. It performs the necessary data and protocol conversion functions as well as many other functions that can be enabled or disabled by the user to meet specific application needs

3.2 Overview

The hardware is structured around a central microcontroller, including on-chip peripherals. The microcontroller utilizes several off-chip peripheral devices: FLASH memory; RAM; FIFOs; serial communications controller (SCC); CAN controller; J1850 VPW DLC device; J1850 PWM HBCC device; a free running 24-bit microsecond clock; and the interface to the host VXI system.

3.3 PC Board

The AVT-512 is a six layer PC board with two full size power and ground planes. These power and ground planes are split which creates an isolated section on the board. In this isolated section are all components (transceivers, data line selection, clock generation, etc.) directly connected to the external vehicle networks. All signals between the isolated and non-isolated (host VXI system) are passed through high speed opto-couplers. Power to the isolated section is provided by both a +5

VDC and a +12 VDC isolated DC/DC converters. The input power to the two DC/DC converters is supplied by the host VXI system.

3.4 Microcontroller

The heart of the AVT-512 M-Module Interface is the Motorola 68332 microcontroller which contains a CPU32 core. The microcontroller contains 2 Kbytes of on-board RAM as well as a number of peripheral functions (chip select, SCI, SPI, TPU, etc.).

The microcontroller currently runs at a bus speed of 16.777 MHz (which may be increased at a later time).

3.5 FLASH

All operational firmware is contained in a 128 Kbyte FLASH (64 K x 16) device that is socket mounted on the AVT-512 M-Module board.

All firmware on the AVT-512 M-Module Interface was developed by and is supported by Advanced Vehicle Technologies, Inc.

The AVT-512 M-Module Interface supports the ability to upgrade operational firmware in the field, without requiring the removal/replacement of the FLASH device. Firmware routines exists in the FLASH device to permit updating the AVT-512 operational firmware from the host computer; without requiring the removal/replacement of the FLASH device.

AVT plans to develop and make available an AVT-512 FLASH programming application for host computers. That application would then permit users to load the AVT-512 FLASH device with updated operational firmware.

3.6 RAM

8 Kbytes (8 K x 8) of RAM are provided by an external RAM device.

3.7 FIFOs

Two high speed hardware FIFOs are used by the microcontroller as buffers for data moving between itself and the host computer. Each FIFO is 2 Kbytes deep. One is used for incoming data (from the host) and the other is used for outbound data (to the host).

[FIFOs are available up to 64 Kbytes deep and may be utilized in the future to provide additional buffering space - especially for FIFO #2, the outbound FIFO, for moving large quantities of data from the vehicle network, through the AVT-512, and to the host.]

3.8 SCC

The “A” half of a Philips Serial Communications Controller (SCC) is used to implement the data link layer (UART) function of Keyword Protocol 2000 [ISO 14230].

The K-line transceiver is implemented using an Advanced Vehicle Technologies, Inc. proprietary design in discrete components.

There is no L-line transmitter function in hardware revision "B".

The "B" half of the SCC is used to implement the data link layer (UART) function of UBP (UART Based Protocol).

A Motorola UPL (UBP Physical Layer) device is used to provide the transceiver function for UBP.

3.9 CAN

CAN operations are supported by the Intel 82527 CAN Controller device.

There are two physical layer transceivers available; selected by software control:

- 2-wire CAN. The Philips 82C250 transceiver is used.
- SWC (Single Wire CAN). The Philips AU5790 transceiver is used.

3.10 J1850 VPW

J1850 VPW operations are supported by the Motorola DLC device (MC68HC57 or 58). Additionally, the AVT-512 M-Module Interface supports full GM Class 2 operations (block transfer mode, 4X mode, etc.).

3.11 J1850 PWM

J1850 PWM operations are supported through the use of the Motorola HBCC (Hosted Bus Controller Chip) device. Using this device ensures Ford Motor Company SCP operational compliance. The physical layer transceiver is implemented in discrete components in accordance with Ford Motor Company design specifications.

3.12 Microsecond Clock

The AVT-512 M-Module Interface utilizes a free running 24-bit microsecond clock for all time related functions. This includes message time stamps and byte and message time intervals in both Keyword Protocol 2000 mode and UBP mode (both of which are heavily time dependent for proper operations).

The clock tick interval is 1.0 microsecond. The clock rolls over at $00 FF FF FF. The rollover interval is 16.777 216 seconds.

3.13 Power Supplies

Note: The ground pins on P3 (pins #4 and #5) are isolated and separate from the host chassis ground. Do not permit isolated ground and host chassis ground to be tied together.

The AVT-512 M-Module requires +5 VDC and nominal +12 VDC power sources.

The +5 VDC is required for all of the digital circuitry on the AVT-512 board and is supplied by the host VXI system.

The +12 VDC supply is the nominal vehicle battery supply and is required to support two modes of operation; KWP and UBP. It is only used for the physical layer transceiver functions. The +12 VDC supply is jumper selected. Refer to Sections 6.3.8, 6.3.9, and 6.3.10 for information on setting the jumpers. Note that the two supplies are diode isolated. Both may be connected, but the higher voltage source will be selected and routed to the transceivers.

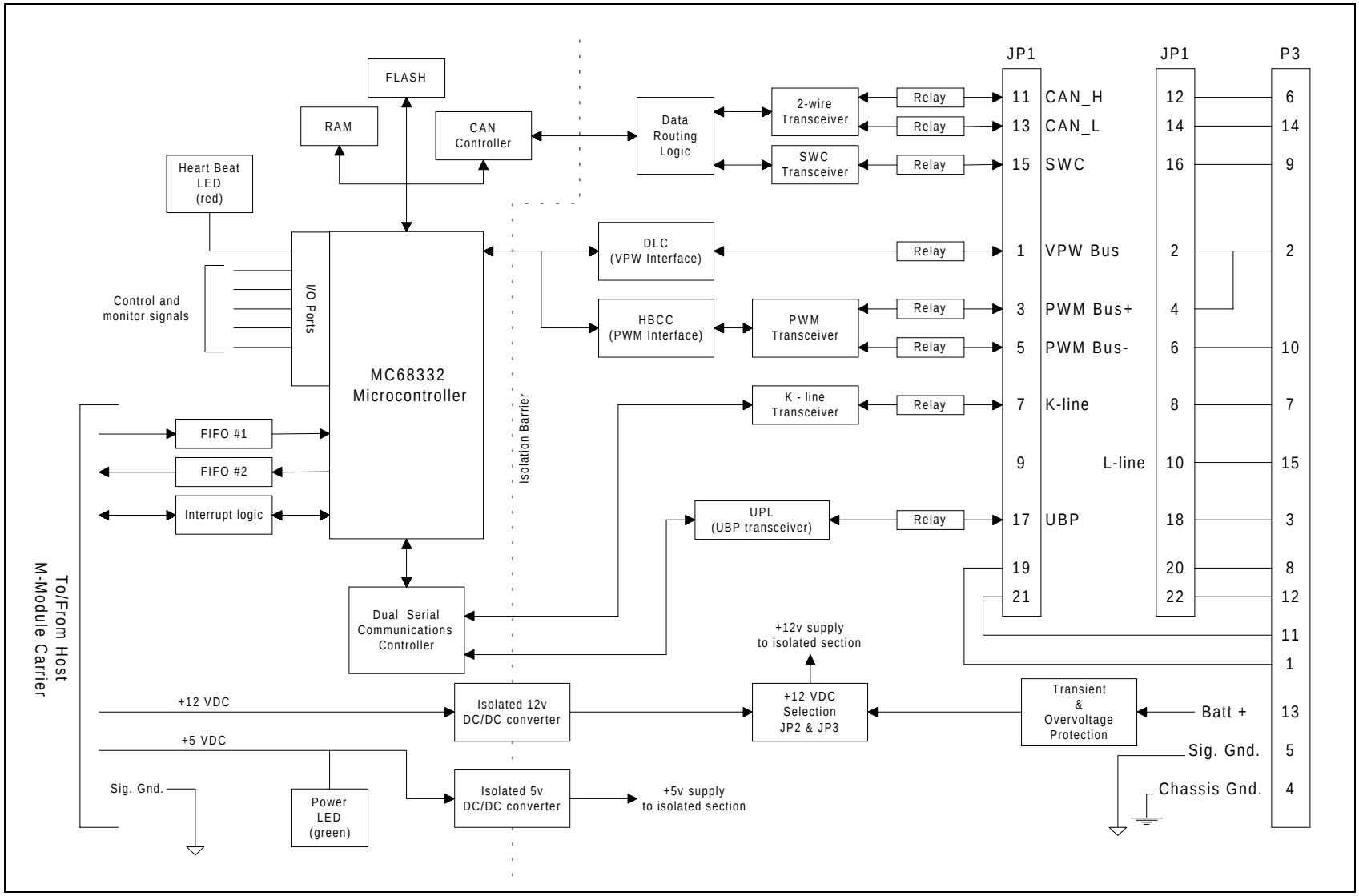

Figure 1 AVT-512 M-Module Interface Block Diagram

4. AVT-512 Operation

The following describes the use of the AVT-512 M-Module Interface. It is assumed that:

- The AVT-512 is properly configured.
- The AVT-512 is properly installed onto an M-Module carrier board.
- The M-Module carrier board is properly configured.
- The M-Module carrier board is properly installed into a suitable chassis.
- The host chassis is functional and connected in some manner to a host computer.
- Communications between the host computer and AVT-512 M-Module Interface have been successfully tested, as described in Section 2.5 and 2.6.

4.1 Indicators

The AVT-512 M-Module board has two indicator LED's: one green and one red.

The green LED is connected to the +5 VDC supply on the board and provides a quick indication that power is present. If the green LED should fail to light, check the power source from the host carrier board and VXI system. The +5 VDC source is protected by F5 on the AVT-512 M-Module board.

The red LED is a heartbeat indicator. The microcontroller toggles the state of the red LED every 62.5 milliseconds during normal operations.

During FLASH programming mode, the red LED will flash on one second intervals.

If a problem with the microcontroller should occur the red LED will, most likely, go to a full ON or full OFF state. This should be readily apparent and be indicative of an abnormal condition.

4.2 Host Interface

All communications between the AVT-512 M-Module Interface and the host computer is performed by reading and writing to the two hardware FIFOs, one status register, and one control register.

All registers, signals, and bits are defined below. Usage, issues and examples are also provided.

4.2.1 Register Definitions

The AVT-512 M-Module Interface is a memory mapped device. The AVT-512 is accessed through a set of registers which are defined in Table 1. The following notes apply to the AVT-512 M-Module Interface:

- ⇒ Offset addresses are shown in hex.
- ⇒ All accesses are byte sized.
- ⇒ All accesses are odd addresses [/DS0 active].
- ⇒ Read and/or write as indicated.
- ⇒ All other locations are undefined and not used.

Register Name	**Offset (hex)**	**Access**	**Notes**
CONTROL	$11	write only	only bit 7 is active bit 7 = '0' AVT-512 is enabled bit 7 = '1' AVT-512 is disabled all other bits are ignored
STATUS	$11	read only	all bits are defined in Section 4.2.2 Table 2
FIFO #1	$15	write only	write to FIFO #1 to send a byte to the AVT-512 board
FIFO #2	$19	read only	read from FIFO #2 to read a byte from the AVT-512 board
IRQ CLEAR	$21	write only only bit 0 is active	write bit '0' = 0 to clear a pending interrupt
AVT-512 board EEPROM	$FE	read and write	implemented as defined in ANSI/VITA 12-1996

Table 1 Register Definitions

4.2.2 Status Register Bit Definitions

The STATUS register bit definitions are listed in Table 2.

Bit #	Definitions
bit 7	/RUN_STATUS flag '1' = the AVT-512 board is enabled to run '0' = the AVT-512 board is disabled
bit 6	"/END_OF_PACKET" status flag '0' = a complete packet has been written into FIFO #2 '1' = not active
bit 5	"/FIFO_2_FULL" status flag '0' = FIFO #2 is full '1' = FIFO #2 is not full
bit 4	"/FIFO_2_EMPTY" status flag '0' = FIFO #2 is empty '1' = FIFO #2 is not empty
bit 3	not used always returns a '1'
bit 2	"/FIFO_1_FULL" status flag '0' = FIFO #1 is full '1' = FIFO #1 is not full
bit 1	"/FIFO_1_EMPTY" status flag '0' = FIFO #1 is empty '1' = FIFO #1 is not empty
bit 0	Module "/IRQ" status flag '0' = Module IRQ is active. '1' = not active

Table 2 Status Register Bit Definitions

4.2.3 AVT-512 RUN Status Flag

On power-up the AVT-512 comes up running, as indicated by the flashing red heartbeat LED. The user application can monitor the /RUN_STATUS of the AVT-512 microcontroller by examining the state of bit # 7 in the STATUS register.

The application can also control the state of the AVT-512 microcontroller by writing to CONTROL register, bit #7. Writing a '0' in bit #7 of the CONTROL register sets the AVT-512 microcontroller to the RUN enabled state and enables the AVT-512 for operations. Writing a '1' in bit #7 of the

CONTROL register halts the AVT-512 microcontroller and disables the AVT-512 unit from operations.

Note that the relationship between bit 7 of the control register (RESET_COMMAND) is opposite to that of the /RUN_STATUS, bit 7, of the Status register.

4.2.4 END_OF_PACKET Status Flag

Bit #0 in the STATUS register is the /END_OF_PACKET status flag. It is an active low flag that is driven true (low) by the AVT-512 unit when a complete packet has been written into FIFO #2 and is ready for the host to read.

The /END_OF_PACKET status flag is tied to the interrupt request line on the AVT-512 M-Module. If the interrupt function is enabled on the AVT-512 board, an interrupt will be generated at the same time as the /END_OF_PACKET flag is driven active (low). If the interrupt function is disabled, no interrupt will be generated.

The /END_OF_PACKET flag is latched and will remain active (low) until any one of the following occur, at which point the flag will be set to '1':

- The host application writes a '0' in bit #0 of the IRQ_CLEAR register.
- The host conducts an interrupt acknowledge cycle for types "B" or "C" interrupts.
- The host activates the master RESET line (a host chassis function).

4.2.5 Module IRQ Status Flag

System Interrupt Request: "IRQ".
Bit #0 in the STATUS register is the /IRQ status flag. This bit reflects the state of the AVT-512 module IRQ line to the carrier board. It is an active low flag that is driven true (low) by the AVT-512 unit when it is asserting an IRQ to the host system.

The /IRQ flag is latched and will remain active (low) until any one of the following occur, at which point the flag will be set to '1':

- The host application writes a '0' in bit #0 of the IRQ_CLEAR register.
- The host conducts an interrupt acknowledge cycle for types "B" or "C" interrupts.
- The host activates the master RESET line (a host chassis function).

4.2.6 Polling Operations

There are two strategies available when using the AVT-512 in a polling environment.

A. Read the STATUS register and test bit # 4. If bit #4 is '0' then FIFO #2 is empty and there is no data to be read. If an empty FIFO is read the data will not be valid and will be indeterminate.

   This is the most common implementation for reading data from the AVT-512 board. The user should be aware that each read from FIFO #2 should be preceded by checking

the status of the FIFO #2 EMPTY FLAG to prevent reading invalid data.

It is possible that the host application could start reading FIFO #2 while the AVT-512 is writing the packet into the FIFO. In that case the host application routine will have to wait for each byte until the complete packet has been read. Other techniques can be implemented where the available bytes are read from FIFO #2, the read routine exits and returns at a later time to finish reading the packet started previously.

B. An alternate method is available that uses the /END_OF_PACKET flag. Each time the polling routine is entered, read the state of the /END_OF_PACKET flag. If it is true (low or '0') then at least one complete packet is available in FIFO #2. Clear the /END_OF_PACKET flag, read the packet from FIFO #2, test the status of FIFO #2 empty flag, if not empty read the next packet from FIFO #2 (if available), test the status of the /END_OF_PACKET flag, if true, read the next packet (or wait until the next polling loop).

Both methods have benefits and drawbacks. These notes are only provided here to give the user some initial ideas.

4.2.7 Register Setup Examples

The example provided here is for setting up the AVT-512 for direct I/O in Agilent VEE, version 5.01.. (The Agilent VXI Resource Manager is used. [Agilent VISA])

- Ensure the AVT-512 is properly installed onto the M-Module carrier board.
- Ensure the Logical Address on the carrier board is set properly and for the proper M-Module location occupied by the AVT-512 unit. Note that only connector P5 on the AVT-512 is active. Refer to Sections 6.3.13 and 6.3.14 for more information.
- Turn on the host chassis. Observe on the AVT-512 that the green LED is on and the red LED is flashing fast.
- In VEE: select the I/O pull down menu. Select INSTRUMENT MANAGER.
- Select and highlight the VXI chassis icon. Select FIND INSTRUMENTS. A NEW DEVICE will appear. Check that it is the address of the AVT-512 M-Module Interface, just installed.
- Select the NEW DEVICE to highlight it.
- Select EDIT INSTRUMENT. In the DEVICE CONFIGURATION window select ADVANCED I/O CONFIGURATION.
- Select the A24/A32 SPACE page.
- Select ADD LOCATION. Add a location for each register defined in Section 4.2.1. Be sure to fill in NAME, OFFSET, FORMAT, and MODE accurately for each register defined in Section 4.2.1.
- Close each window, in succession, by selecting OK and thus saving the configuration defined for the AVT-512 M-Module Interface.

At this point the AVT-512 M-Module Interface is defined for use in Agilent VEE.

Some Agilent VEE routines may be available from Advanced Vehicle Technologies. Contact the factory for more information.

4.2.8 Interrupts

The AVT-512 M-Module Interface supports all three interrupt types as defined in the M-Module specification, ANSI/VITA 12-1996. They are known as Type “A”, “B”, and “C”.

If enabled the AVT-512 can generate an interrupt each time it finishes writing a complete packet to FIFO #2. This results in an interrupt each time a complete packet is waiting in FIFO #2 for the host to read. The user should be aware that the AVT-512 could write more than one packet into FIFO #2 while the interrupt is active and waiting for service. Other scenarios are equally likely.

Upon power up, the AVT-512 will not generate an interrupt. This function must be enabled each time the AVT-512 comes out of a reset (hardware or software reset). The interrupt function is enabled or disabled through the use of the `"$52 $2E $xx"` command (xx = 00 disables the interrupt function and xx = 01 enables the interrupt function).

Type “A” interrupts require that the host write a value of bit 0 = ‘0’ to the “IRQ_CLEAR” register to clear the interrupt. This is known as a RORA (Release On Register Access) interrupt.

Type “B” interrupts are cleared by the host activating the /IACK line. When /IACK is pulsed active (low) the interrupt being generated by the AVT-512 is automatically cleared.

Type “C” interrupts are cleared during the interrupt acknowledge cycle. During this cycle the host performs a read operation with the exception that the /IACK line is active during the read cycle but the /CS line is not. During the interrupt acknowledge cycle the AVT-512 places the current value of the STATUS register onto the low order data lines (DATA 07..0).

When using the Agilent E2251A M-Module carrier board, the current value of the STATUS register will show up at the host on the high order data bits [DATA 15...08] and the logical address of the AVT-512 M-Module generating the interrupt will be on the low order data bits [DATA 07...00].

Type “C” interrupts are known as ROAK (Release On AcKnowledge) interrupts.

4.2.9 On-Board EEPROM Configuration Information

On power-up the host chassis queries the AVT-512 M-Module and looks for the presence of an EEPROM containing configuration information. If that EEPROM is found, the host reads it and uses it to configure the system environment and/or store the information for user access.

The AVT-512 M-Module uses an EEPROM, as defined in ANSI/VITA 12 (and expanded upon by Agilent). The contents and definitions of the contents of the EEPROM on the AVT-512 are defined here.

Location [word address]	**Definitions**
$00	sync code, $5346
$01	module number, $06A5, (1701 decimal)
$02	revision level, $0001
$03	module characteristics, $1861 bit 15: 0 - no burst access bit 14: 0 - reserved bit 13: 0 - reserved bit 12: 1 - module does need +12 VDC (-12 is not used on the AVT-512) bit 11: 1 - module does need +5 VDC bit 10: 0 - module does not have trigger outputs bit 09: 0 - module does not have trigger inputs bits 08 07: 00 - not a DMA requester bits 06 05: 11 - interrupter type "C" bits 04 03: 00 - 8-bit data bus bits 02 01: 00 - 8-bit address bus bit 00: 1 - module supports memory access
$04 to $07	reserved, all $0000
$08 to $0F	user defined, all $FFFF
$10	sync code, larger EEPROM, $ACBA
$11	VXI ID, $CE67, (3687 decimal), Advanced Vehicle Technologies, Inc. [Upper nibble is $C; the module has A16 and A24 space and is a register device.]
$12	VXI device, $F200, (512 decimal), M-Module model number [Upper nibble is $F; it requires 256 bytes of A24 space.]
$13	VXI device, $08FD, (2301 decimal)

Table 3 AVT-512 EEPROM Contents

4.2.10 VXIplug&play Drivers

VXI*plug&play* drivers are under development at the time of this writing. Contact the factory for the latest information on the availability of VXI*plug&play* drivers.

4.2.11 Soft Front Panel

The soft front panel is part of the VXI*plug&play* drivers. Contact the factory for the latest information on the availability of VXI*plug&play* drivers and soft front panel.

4.3 Vehicle Networks

All communications between the AVT-512 M-Module Interface and the external vehicle networks were designed to be in conformance with all relevant standards and specifications.

5. Communications

The structure and protocol of communications between the AVT-512 M-Module Interface and the host computer are stated in the following sections.

5.1.1 Packet Construction

All communications between the AVT-512 M-Module and the host computer are accomplished in "packets."

Packets from the host computer to the AVT-512 M-Module are known as Commands.

Packets from the AVT-512 M-Module to the host computer are known as Responses.

All data is transferred in packets. The size of each data packet varies depending on the mode of operation. For most modes the packet length is from 1 to 16 bytes (inclusive) but may be as much as 260 bytes in KWP mode and much larger in VPW block transfer mode.

The first byte in each data packet is called the HEADER BYTE and is used to convey information only between the control computer and the AVT-512 M-Module.

The header byte is divided into the upper nibble and lower nibble. The upper nibble indicates what information the data packet is conveying. The lower nibble is the count of the number of bytes that follow the header byte. The meaning of the upper nibble of the header byte depends on which direction the data packet is moving; whether to or from the control computer.

There are occasions where packets between the AVT-512 M-Module and the host computer are more than 15 bytes in length. To support these longer packets, two alternate forms have been developed. Refer to Section 5.1.7 of this manual and/or refer to the document "Long Messages - Alternate Header Formats."

5.1.2 Transmit message format

To transmit a message onto the network the message must be built by the operator and then sent to the AVT-512 M-Module.

The CRC or checksum byte will be automatically calculated and appended onto the message when transmitted. In some operational modes this function can be enabled or disabled by software command.

Any message destined for transmission must be preceded by a byte whose upper nibble is '0' (zero) and lower nibble is the byte count of the message (unless one of the alternate header forms is used). The message bytes then follow immediately.

It is up to the user to determine and know the proper messaging strategy that is used on the external network to which the AVT-512 M-Module is attached.

5.1.2.1 Transmit Acknowledgment

Each time a message transmission is attempted the interface will issue some kind of transmission acknowledgment. The type and meaning of this transmission acknowledgment is dependent on the mode of operation.

For VPW and KWP modes, the transmit status byte definition is the same as the receive message status byte.

CAN mode does not have a transmit status byte.

PWM does not have a transmit status byte, but the AVT-512 M-Module will forward any received acknowledgments to the host computer.

In UBP mode of operation, when a message is transmitted onto the network, the AVT-512 M-Module will issue a receive message report to the host, along with a status byte. The AVT-512 M-Module will also issue a separate transmit status report.

Some operational modes permit the user to enable or disable the function "Forward messages from this device." When enabled, the host receives a complete copy of the message just transmitted, with the status bits set accordingly. When disabled, the host receives just the status byte (for example, 01 60).

Refer to the "Master Command and Responses" document for detailed information on each specific mode of operation.

5.1.3 Transmit Message Status Byte Definitions

Refer to the "Master Commands and Responses" document for exact bit definitions of the status byte that accompanies the transmit acknowledgment.

5.1.3.1 Transmit message example

The user has set the AVT-512 M-Module to VPW mode.
The user wants to send the following OBD-II Mode 01 PID 00 query: 68 6A F1 01 00.

The user assembles and sends the following packet to the AVT-512 M-Module Interface:

05 68 6A F1 01 00.

After the AVT-512 M-Module Interface has transmitted the message onto the network, successfully, the user receives the following at the host computer:

01 60

5.1.4 Receive message format

Messages received from the network are assembled into the original byte sequence. The received CRC or checksum is calculated and checked to be equal to the CRC or checksum byte at the end of the received message. The received status byte is updated and the entire packet is sent to the host.

Depending on the mode of operation, the received CRC/checksum byte is discarded or preserved according to command $52 $01 $xx. (In VPW and CAN mode the CRC/checksum byte is always discarded.)

Some modes of operation enforce format checking rules to the received message (even if it was transmitted by the AVT-512 M-Module). The user should consult the appropriate specifications and related documents for details on the format of messages in specific modes of operation.

Status of all such tests are indicated in the received status byte.

5.1.4.1 Received message time stamping

All modes of operation support received message time stamping. This function is enabled or disabled by the user through the use of the 5x 08 command.

If time stamps are disabled (default setting), then the format of a received message is:

- ◊ Header byte(s); 1 to 3 bytes.
  (Depending on the packet size, one of the alternate header formats may be used.)
- ◊ Received status byte; 1 byte.
- ◊ Message bytes ...

If time stamps are enabled, then the format of a received message is:

- ◊ Header byte(s); 1 to 3 bytes.
  (Depending on the packet size, one of the alternate header formats may be used.)
- ◊ Time stamp; 4 bytes.
- ◊ Received status byte; 1 byte.
- ◊ Message bytes ...

5.1.4.2 Received message example

As an example the byte sequence $A7 $B6 $C5 plus CRC/checksum byte appears on the network. The message is received by the AVT-512 M-Module and the following byte sequence is passed to the host computer: $04 $00 $A7 $B6 $C5 (time stamping is disabled).

The byte $04 indicates that it is a received message and that four bytes follow.
The byte $00 is the received message status byte and indicates that no errors were found.
(Received message status byte, bit definitions are listed in the next section.)
The message bytes then follow. Note that the CRC or checksum byte is stripped off.

5.1.5 Received Message Status Byte Definitions

The user should consult the "Master Commands and Responses" guide for the most up-to-date listing of the bit definitions for the received message status byte for each mode of operation.

5.1.6 More Examples

To illustrate the construction and decoding of packets between the control computer and the AVT-512 M-Module, several examples are provided.

Example #1: Want to request the current operational mode.

Command: `D0`.
The AVT-512 M-Module Interface responds with: `91 14`.
The '`9`' indicates a board status response.
The '`1`' indicates one byte follows
The `14` indicates UBP mode.

Example #2: want to send a message out on the bus.

Command: `04 32 89 AC 5F`.
The AVT-512 M-Module responds with: `01 40`.
The '`0`' indicates a received message from the network.
The '`1`' indicates only one byte follows. The one byte is the received message status byte.
The '`40`' is the received message status byte with bit `6` only being set.
Bit `6` is set. This means the received message was 'from this device' meaning the AVT-512 M-Module unit.

Messages transmitted by the AVT-512 M-Module are received by the AVT-512.
They are checked for errors.
Unless otherwise configured, only the status byte is sent to the host

In UBP mode, the AVT-512 M-Module will also send the transmission acknowledgment `A1 60` which indicates that the message was successfully transmitted.

5.1.7 Alternate Header Formats

There are occasions where packets between the AVT-512 M-Module and the host computer are more than 15 bytes in length. To support these longer packets, two alternate forms have been developed. The user may also refer to the document "Long Messages - Alternate Header Formats."

To accommodate long messages, the format for communications between the AVT-512 M-Module unit and the host computer has been modified. The host has three methods available for

passing a packet to the AVT-512 M-Module for transmission onto the vehicle network. All three methods are described here, along with examples.

If the message is 15 bytes or less in length (total) then the 'normal' format may be used.

Normal Format: 0x aa bb cc ...
x - count of bytes to follow
aa bb cc ... message bytes.

Example: 05 81 F1 C1 48 9B

If the message is more than 15 bytes but less than 255 bytes in length, alternate format #1 is available using a header byte of $11.

Alternate format #1: 11 xx aa bb cc ...
11 - header byte
xx - count of bytes to follow
aa bb cc ... message bytes.

If the message is more than 255 bytes in length, alternate format #2 is available using a header byte of $12.

Alternate format #2: 12 xx yy aa bb cc ...
12 - header byte
xx - count of bytes to follow, most significant byte
yy - count of bytes to follow, least significant byte
aa bb cc ... message bytes.

These formats are backward compatible and may be used as desired.

For example, the host wants to transmit the following message onto the bus:

A1 B2 C3 D4 E5 F6 A7 B8 C9 DA EB FC AD BE

The following messages from the host to the AVT-512 M-Module are all equivalent. The header byte(s) have been bolded and underlined for clarity.

0E A1 B2 C3 D4 E5 F6 A7 B8 C9 DA EB FC AD BE

11 0E A1 B2 C3 D4 E5 F6 A7 B8 C9 DA EB FC AD BE

12 00 0E A1 B2 C3 D4 E5 F6 A7 B8 C9 DA EB FC AD BE

5.2 VPW Mode

Consult the latest version of the “Master Commands and Responses” document for detailed information on the commands supported by the AVT-512 M-Module Interface while in VPW mode of operation.

The latest version of the “Master Commands and Responses” document can be obtained from our web site at: http://www.avt-hq.com

When in VPW mode of operation the interface is always listening to, or monitoring, the external network. All bus traffic is reported to the control computer by the interface. Transmit operations occur only when initiated by the control computer.

5.3 PWM Mode

Consult the latest version of the "Master Commands and Responses" document for detailed information on the commands supported by the AVT-512 M-Module Interface while in PWM mode of operation.

The latest version of the "Master Commands and Responses" document can be obtained from our web site at: http://www.avt-hq.com

When in PWM mode, there are two sub-modes of operation: "Active Node" and "Passive Node." These two sub-modes of operation are due to the peculiarities of the HBCC device.

5.3.1 PWM Active Node

When PWM mode is first entered, or the HBCC is commanded to reset, the AVT-512 initializes the HBCC device, conducts an internal test, and then connects to the external network.

Unlike VPW mode, the HBCC device does not receive messages it sends. The AVT-512 M-Module interface will not send a transmission acknowledgment to the host.

PWM operations are unique in that all transmitted messages must be acknowledged by at least one receiving node (not itself). The node that acknowledges receipt of a message does so by placing it's node address in the IFR field of the network message. The AVT-512 will respond to the host with the address of the responding node or nodes to every message transmitted.

The HBCC device also filters all received network messages. The host will only 'see' network messages that are either physically addressed to the AVT-512 or messages that have matching entries in the 'function message' or 'function read message' look-up tables. The AVT-512 initializes the HBCC with a node address of $F1. Additional information on HBCC initialization can be found in the AVT document: "HBCC Initialization Parameters" available from our web site. Also of interest might be the AVT document: "HBCC (PWM) Interrupt Register Definitions."

One other important point is that in default mode of operation, the HBCC, thus the AVT-512, the user should omit the source ID byte in any message to be transmitted. When transmitting a message the HBCC automatically inserts its node address as the third byte (source byte) of the message being transmitted.

As an example, in PWM mode, the OBD-II Mode 01 PID 00 request is: $61 $6A $F1 $01 $00. To send this message onto the network the host sends to the AVT-512, through FIFO #1, the following: $04 $61 $6A $01 $00. Note that the source address, $F1, is omitted. The HBCC will automatically insert that byte as well as compute and transmit the correct CRC byte at the end of the message. Successful receipt of that message by another module is causes the AVT-512 to issue to the host the transmit acknowledgment packet: "$A1 $10" indicating that a module with physical address of $10 received the message.

The AVT-512 does not generate a “Received Status Byte” for each received message. The byte immediately following the header byte indicates the table entry number the message matched, referring to the ‘function’ and ‘function read’ message lookup tables. The host is notified by the AVT-512 of any errors detected when transmitting or receiving a message from the network by using a separate error message (a $2x xx xx type of message).

5.3.2 PWM Passive Node

The HBCC can be configured to monitor the PWM network. As such it becomes a passive network node and will not transmit a received message acknowledgment. In this configuration the HBCC is not permitted to transmit any messages. Additionally, message filtering is disabled and all messages that show up on the network, including the transmit acknowledgments, are received and passed to the host computer.

To enable passive network monitoring send the following command to the AVT-512 unit:

```
$83 01 02 16
```

To disable passive network monitoring and return to active node status, either reset the HBCC device using the $21 01 command, or send the following command to the AVT-512 unit:

```
$83 01 02 72
```

5.4 KWP Mode

Consult the latest version of the “Master Commands and Responses” document for detailed information on the commands supported by the AVT-512 M-Module Interface while in KWP mode of operation.

The latest version of the “Master Commands and Responses” document can be obtained from our web site at: http://www.avt-hq.com

Note that since the AVT-512 M-Module supports operations in Keyword Protocol 2000 mode, it will support ISO 9141 and ISO 9141-2 operations. CARB mode initialization should be used.

The AVT-512 M-Module Interface does not provide “L-line” support.

Operations in KWP mode are slightly different than in VPW mode.

When first entering KWP mode, the AVT-512 M-Module is disconnected from the network (K-line). There are two ways to connect to the network.

1. Conduct a communications initialization with the vehicle. The AVT-512 M-Module supports all three methods, as required by the ISO 14230 specification. The three initialization methods are mentioned here. Consult the document “Keyword Protocol 2000 Initialization” for detailed information about each of these initialization sequences.

    A. CARB mode initialization. This is the mode that should be used for ISO 9141-2 applications; such as OBD-II operations. The command is: $61 11.

B. 5-Baud mode initialization. The command is: $61 12.

C. Fast initialization. The command is: $6x 13 yy zz ...

Note that following successful initialization of the communications link, the AVT-512 M-Module will monitor for transmitted messages. If no transmit activity is sensed within 4.5 seconds the AVT-512 M-Module Interface will automatically transmit a Mode 1 PID 0 request (this is an OBD-II query). This is known as the "Keep Alive" message and is used to keep the communications link open or active. The "Keep Alive" message can be changed or disabled by the user.

2. Issue the $61 04 command. This will shut the K-line relay and connect the AVT-512 M-Module unit to the network K-line. Unless changed by the operator (using the 53 03 xx yy command) the AVT-512 M-Module defaults to the K-line baud rate of 10.4 kbps. Any network traffic will be received by the AVT-512 M-Module and forwarded to the host computer.

5.5 CAN Mode

Consult the latest version of the "Master Commands and Responses" document for detailed information on the commands supported by the AVT-512 M-Module Interface while in CAN mode of operation.

The latest version of the "Master Commands and Responses" document can be obtained from our web site at: http://www.avt-hq.com

Operations in CAN mode are quite different than any other mode. The user is also referred to the AVT document "A Discussion about CAN" for detailed information on CAN operations and the construction of packets between the AVT-512 M-Module and the host computer.

5.6 UBP Mode

Consult the latest version of the "Master Commands and Responses" document for detailed information on the commands supported by the AVT-512 M-Module while in UBP mode of operation.

The latest version of the "Master Commands and Responses" document can be obtained from our web site at: http://www.avt-hq.com

Operations in UBP mode are very similar to operations in VPW mode.

Upon entering UBP mode, the AVT-512 M-Module will monitor for transmitted messages. If no transmit activity is sensed within 4.5 seconds the AVT-512 M-Module will automatically transmit a "Keep Alive" message. The "Keep Alive" message can be changed or disabled by the user.

5.7 Match Function - Message Filtering

A coarse filtering mechanism for messages received from the bus is provided by the AVT-512 M-Module firmware. *The match function is not applicable to CAN mode of operation.* If the match table is cleared (on power-up, reset, or $31 $7B command) all messages received from the network are passed to the host.

When at least one entry is made to the match table, all messages received from the network are checked against the match table. If a match is found the message is passed to the host. If no match is found, the message is discarded, and the host is not notified.

A match table entry is made using the $32 $xx $yy command. The $xx value is the byte position and the $yy value is the byte value. This filtering mechanism is more easily explained by example.

> It is desired to receive all messages (at the host) where the third byte of the message is equal to $F1. Send the command $32 $03 $F1 to the AVT-512 M-Module. To verify the table entry send the command $30. The response will be $42 $03 $F1. The only network messages passed to the host will now be of the form: $zz $xx $F1 $... Note that at the host the message will be $rr $ss $zz $xx $F1 $.. where $rr is the header byte, $ss is the received message status byte, and the message follows.

The match table can hold ten entries where an entry consists of a byte position and a byte value. The byte position refers to where in the network message the match byte is to be compared. The first byte of the message has a byte position value of one.

Ordering of the match table is not important. All table entries are checked until a match is found or the end of the table is encountered. If a match table entry specifies a byte position that doesn't exist for the message being checked (the message is shorter than the table entry), that table entry is not checked.

Note that the header byte and the received message status byte are not included in the match function nor are these two bytes considered part of the message. When in UBP and ISO modes the byte following the header byte is the received message status byte. When in PWM mode the byte following the header byte is the message number. These bytes are ignored by the match function and are not counted. The very next byte is the first byte of the message and has is byte number one of the message.

5.8 Status and Error Codes

Consult the latest version of the "Commands and Responses" list for a complete list of Status and Error codes supported by the AVT-512 M-Module Interface.

The latest version of the "Commands and Responses" document can be obtained from our web site at: http://www.avt-hq.com

6. Technical Information

6.1 Reference Documentation

Listed here are Specifications and other documentation related to the AVT-512 M-Module Interface and the functions which it performs.

1. ANSI/VITA 12-1996 M-Module Specification.
2. SAE Specification J1850.
3. SAE Specification J1979.
4. SAE Specification J2411.
5. ISO 11898
6. ISO 9141.
7. ISO 9141-2.
8. ISO 14230.

6.2 Technical Support

The user may contact Advanced Vehicle Technologies, Inc. for assistance in any of the areas covered here. When calling please be prepared to identify yourself and tell us the serial number of your hardware.

Advanced Vehicle Technologies, Inc. is located in Maryland and is open from 0800 hrs. to 1800 hrs. Eastern Time. If calling after hours, please leave a message and we will return your call as quickly as possible.

You may also fax your questions to us. We will either fax an answer back or call you, at your request. If faxing your question, please include as much relevant information about your question or problem as you can.

We can be contacted:

Voice:	410-798-4038
Fax:	410-798-4308
or by E-mail at:	support@avt-hq.com

6.3 AVT-512 M-Module Interface Hardware Information

The following sections contain information about the AVT-512 M-Module Interface board.

6.3.1 Host Supplied +5 VDC Supply

The host carrier board provides the AVT-512 +5 VDC logic supply (VCC). The host supplied +5 VDC powers all of the logic to the non-isolated section of the AVT-512.

An isolated DC/DC converter (+5 VDC in and out) is powered by the host +5 VDC supply and provides all logic power to the isolated section of the AVT-512.

6.3.2 Host Supplied +12 VDC Supply

The host carrier board provides a +12 VDC supply to the AVT-512. This supply is only used to power an isolated DC/DC converter (+12 VDC in and out). The output of this isolated DC/DC converter is used to supply power to the J1850 VPW transceiver and the Single Wire CAN transceiver. The output of this DC/DC converter may also be used to power the UBP transceiver and the K-line transceiver, depending on the setting of jumpers JP2 and JP3 as well as the voltage level of the external +12 VDC supply.

6.3.3 External +12 VDC or V-BATT Supply

A nominal +12 VDC may be supplied externally via P3, pin #13. This supply is over voltage protected, refer to Section 6.3.7 for more information. This input is enabled by jumper JP3 and is diode isolated from the isolated +12 VDC supply. It is used to supply the K-line transceiver and the UBP transceiver.

6.3.4 Fuse F1

Fuse F1 is a Polyswitch fuse (a PTC device) in the +12 VDC supply line from the host carrier board to the isolated DC/DC converter. It is a Raychem SMD050 part. It is only there to protect the host supply in the event of an extended over correct condition on the +12 VDC supply from the host. It will reset when the over correct condition is removed.

6.3.5 Fuse F2

Fuse F2 is a very fast blow 1 amp fuse in the +5 VDC (VCC) supply from the host. It is designed to protect the host and the AVT-512 in the event of an over correct condition on the +5 VDC supply.

F2 is a 1206 Surface Mount (SMT) device. It is very small and located right next to P4 and P5 (the M-Module to carrier board connectors. Suitable replacement part numbers are:

* LittleFuse, SMF, 1206, very fast acting, 1A, 429 series.
  Digi-Key stock number: F1234CT-ND.
  Allied stock number: 845-7003.
* Cooper Bussman, 3216FF series, 1206, 1A,
  Digi-Key stock number: 283-2444-1-ND.
  Allied stock number: 740-3220.

6.3.6 Fuse F3

Fuse F3 is a Polyswitch fuse (a PTC device) in the K-line to the K-line transmitter. It is there to protect the K-line transmitter in the event of a short to battery condition during transmit operations or other over correct conditions. It will trip (go to a high impedance condition) as the result of an over correct condition. It will reset when the over correct condition is removed.

6.3.7 Fuse F4

Fuse F4 is a very fast blow 250 milliamp fuse in the +12 VDC external supply line (via P3). It is designed to work in conjunction with an over voltage detection circuit to protect the AVT-512 components from an over voltage condition. Protection is provided by a "crowbar" action designed to trip at approximately +32 VDC. In the event the AVT-512 is subject to an input voltage surge, the over voltage or "crowbar" circuit acts to clamp the over voltage condition until such time as F4 blows.

F4 is a 1206 Surface Mount (SMT) device. It is very small and located right next to JP2. Suitable replacement part numbers are:

* Schurter "Micron Guard", 250 mA, Schurter part number: 3410.0022.01,
  Allied stock number: 798-0702.
* LittleFuse, SMF, 1206, very fast acting, 250 mA, 429 series.
  Digi-Key stock number: F1230CT-ND.
* Cooper Bussman, 3216FF series, 1206, 250 mA,
  Digi-Key stock number: 283-2440-1-ND.

6.3.8 Jumper JP1

Jumper JP1 is a 22 pin header that permits assignment of signals to the pins of P3.

JP1 is numbered such that all odd numbered pins are in one vertical row and all even numbered pins are in the other vertical row.

A diagram of JP1 is shown in Figure 2.

The default configuration for JP1 is shown in Figure 3 and listed in Table 1.

A detailed listing for all pins of JP1 is provided in Table 2.

Refer to the AVT-512 M-Module Interface unit block diagram, Figure 1. Included on the block diagram are all signal assignments and pin numbers for JP1 and P3.

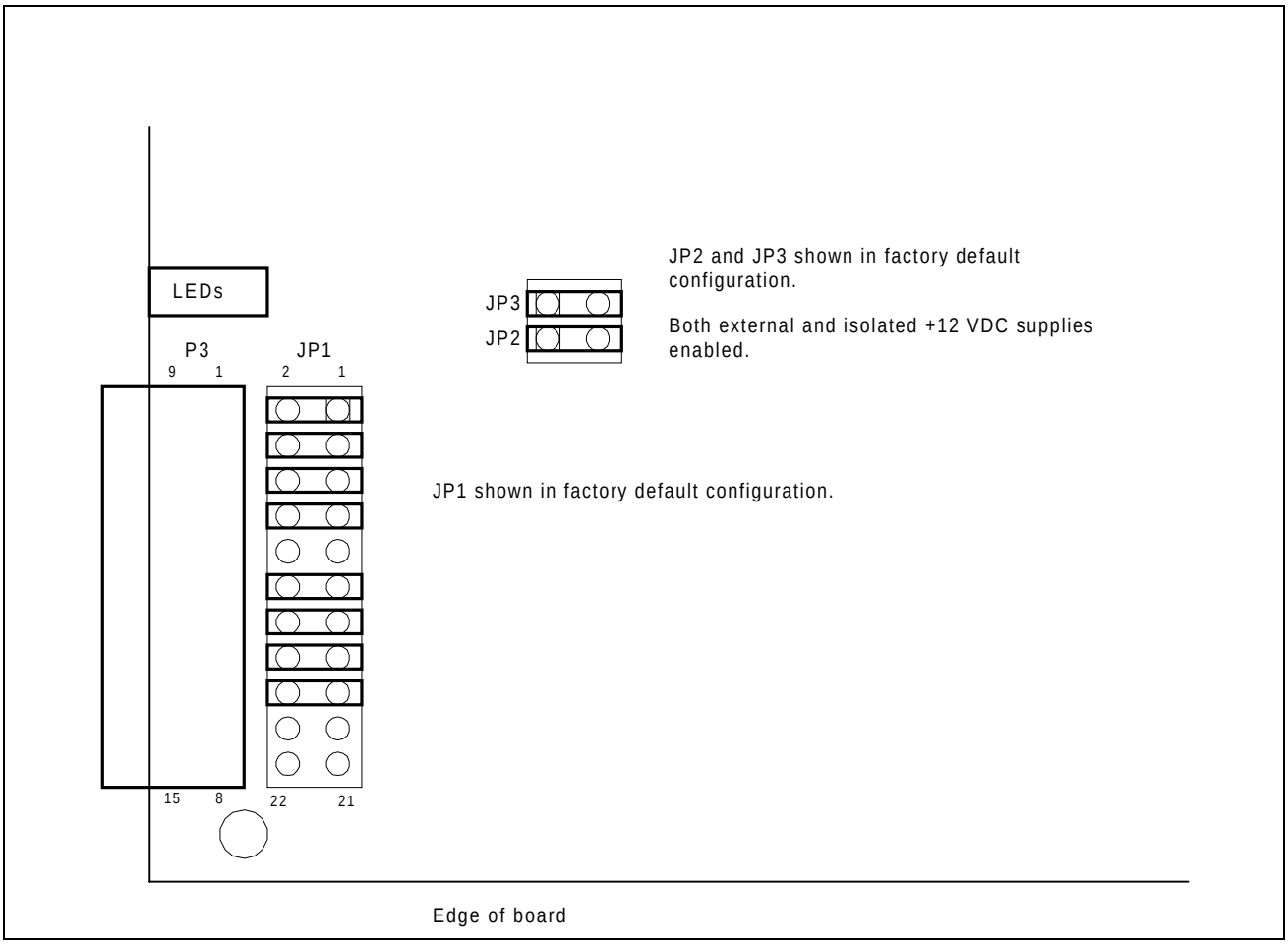

Figure 2 Diagram showing jumper locations

AVT-512 M-Module Interface Signal	JP1 pin #		JP1 pin #	P3 pin #
VPW bus	1	jumper	2	2
PWM bus +	3	jumper	4	2
PWM bus -	5	jumper	6	10
K-line	7	jumper	8	7
	9		10	15
CAN - H	11	jumper	12	6
CAN - L	13	jumper	14	14
SWC	15	jumper	16	
UBP	17	jumper	18	
	19		20	
	21		22	

Table 4 Default Configuration of JP1

AVT-512 M-Module Interface Signal	JP1 pin #		JP1 pin #	P3 pin #
VPW bus	1	jumper	2	2
PWM bus +	3	jumper	4	2
PWM bus -	5	jumper	6	10
K-line	7	jumper	8	7
	9		10	15
CAN - H	11	jumper	12	6
CAN - L	13	jumper	14	14
SWC	15	jumper	16	9
UBP	17	jumper	18	3
P3 pin #1	19		20	8
P3 pin #11	21		22	12

Table 5 Complete Description of JP1

6.3.9 Jumper JP2

When this jumper is installed the external +12 VDC source (from P3 pin # 13) is routed to the diode isolation block and may be used to power the K-line and UBP transceivers. The voltage range for this source is +9 to +30 VDC.

Note that this input voltage source is protected by a “crowbar” over voltage protection circuit and Fuse F4. Refer to Section 6.3.7 for more information.

6.3.10 Jumper JP3

When this jumper is installed the +12 VDC supplied by the isolated DC/DC converter (U23) is routed to the diode isolation block and may be used to power several transceivers (J1850 VPW, single wire can, K-line, and UBP).

The host supplied +12 VDC is routed through fuse F1 and then to the isolated DC/DC converter (U23). Refer to Section 6.3.2 for more information.

6.3.11 Connector P1

Connector P1 exists on the AVT-512 M-Module Interface board to support development, test, and debugging operations. It may not be installed. **Do not connect anything to P1.**

6.3.12 Connector P3

Connector P3 on the AVT-512 M-Module Interface board is a DA-15P connector and will mate to any industry standard DA-15S connector. It can be connected to a vehicle OBD-II connector through an optional OBD-II cable (AVT order number 101-002).

CAUTION

The user should be aware of possible signal conflicts between the AVT-512 M-Module Interface and the vehicle J1979 (OBD-II) connector.

Damage may result to either or both the AVT-512 M-Module Interface and the vehicle if improper signals are connected.

The AVT-512 M-Module Interface supports more protocols than called out in the OBD-II specification (SAE J1979). As such the user should exercise extreme caution when connecting the AVT-512 M-Module Interface directly to a vehicle. The J1979 specification only assigns some of the 16 pins on the OBD-II connector to specific and known signals. All other pins are used by the manufacturer at will.

There may be signal conflicts that could result in damage to the AVT-512 M-Module and/or vehicle. It is for this reason that JP1 is available on the AVT-512 board - the user can change the signal to pin configuration on the AVT-512 to match the vehicle signal pin-out on the OBD-II connector.

Refer to Section 6.3.8 for additional information about JP1.

Refer to the AVT-512 M-Module Interface unit block diagram, Figure 1. Included on the block diagram are all signal assignments and pin numbers for JP1 and P3.

P3 Pin #	Where to	Description	OBD-II Connector [using AVT OBD-II cable]
1	JP1 pin 19		
2	JP1 pin 2 JP1 pin 4		J1850 bus +
3	JP1 pin 18		
4	*isolated ground plane*	Ground	Ground
5	*isolated ground plane*	Ground	Ground
6	JP1 pin 12		
7	JP1 pin 8		K-line
8	JP1 pin 20		
9	JP1 pin 16		
10	JP1 pin 6		J1850 bus -
11	JP1 pin 21		
12	JP1 pin 22		
13	*power input protection circuit*	+V-battery	+V-battery
14	JP1 pin 14		
15	JP1 pin 10		L-line

Table 6 Connector P3

6.3.13 Connector P4

P4 mates to the host M-Module carrier board. Only pins P4B-1, P4B-5, and P4B-8 are connected to the AVT-512 ground plane.

6.3.14 Connector P5

P5 provides the connections for all signals between the AVT-512 M-Module and the host M-Module carrier board. The following signals are connected and used.

Pin #	Signal		Pin #	Signal
P5A-1	/Chip_select		P5B-1	ground
P5A-2	ADDR1		P5B-2	host +5 VDC
P5A-3	ADDR2		P5B-3	host +12 VDC
P5A-4	ADDR3		P5B-5	ground
P5A-5	ADDR4		P5B-8	ground
P5A-6	ADDR5		P5B-9	DATA0
P5A-7	ADDR6		P5B-10	DATA1
P5A-8	ADDR7		P5B-11	DATA2
P5A-18	/DTACK		P5B-12	DATA3
P5A-19	/IACK		P5B-13	DATA4
P5A-20	/RESET		P5B-14	DATA5
			P5B-15	DATA6
			P5B-16	DATA7
			P5B-17	/DS0
			P5B-18	/WR
			P5B-19	/IRQ
			P5B-20	SYSCLOCK

7. Company Overview

Advanced Vehicle Technologies, Inc. is dedicated to providing affordable hardware, software, and technical support to the developers and users of vehicle based networks.

AVT, Inc. also offers other vehicle network products including:

- AVT-718 Multiple Interface unit. Supports: CAN (both 2-wire and SWC), J1850 VPW, J1850 PWM, Keyword Protocol 2000, and UBP. (RS-232 unit).
- AVT-717 CAN and UBP interface. Supports: CAN (both 2-wire and SWC) and UBP. (RS-232/422 unit).
- AVT-716 Multiple Interface. Supports: J1850 VPW, PWM, ISO 9141, KWP2000, ALDL, CCD. (RS-232/422 unit).
- AVT-715 Dual J1850 Interface. Supports: J1850 VPW and J1850 PWM. (RS-232/422 unit)
- AVT-921 Dual J1850 Interface (an 8-bit ISA board).
- AVT-931 Dual J1850 Interface (PC/104 form factor).
- AVT-932 Dual J1850 Interface with Ethernet connectivity (PC/104 form factor).
- AVT-1850-1 J1850 VPW Development System.

Consult our web site and/or contact the factory for information about all of our products.

The engineering staff at AVT, Inc. is experienced with multiplex bus standards including: J1850 VPW, PWM, ISO-9141, ISO-9141-2, Keyword Protocol 2000, ALDL, CCD, CAN, UBP, and more. A design engineer is available to provide assistance on the use of any of AVT's products.

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Revision Record:

A1: Original release. Hardware revision "A" boards only.
B1: Original release. Hardware revision "B" boards only.